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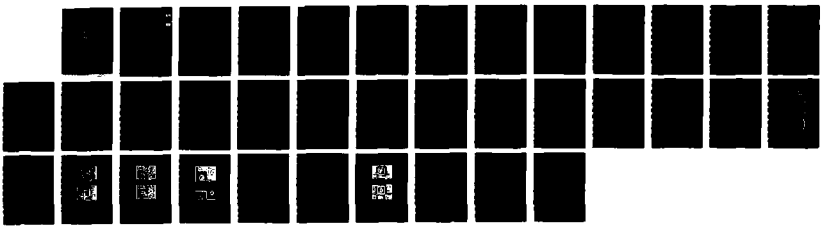

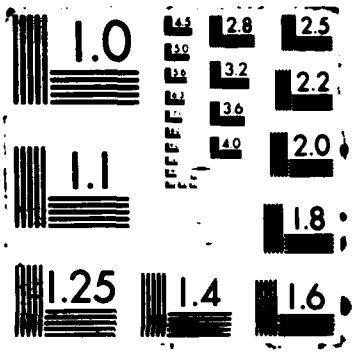
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Two-Dimensional Thermal Oxidation of Silicon
I. Experiments

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Abstract

With continued miniaturization and the development of new devices, the highly nonuniform oxidation of two-dimensional nonplanar silicon structures is playing an increasingly important role. An understanding of this subject has been limited by insufficient experimental data and difficulties in two-dimensional numerical simulation.

This paper introduces a unique experimental approach in which extensive data were obtained concerning the oxidation of cylindrical silicon structures of controlled radii of curvature. It is quantitatively demonstrated that the oxidation of curved silicon surfaces is retarded at low temperatures and sharp curvatures, and that the retardation is more severe on concave than convex structures. These observations will be interpreted using a physical model based on stress effects on oxide growth parameters. The theoretical analysis and modeling will be reported in detail in a separate paper[1].

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1 Introduction

The thermal oxidation of silicon has played an important role in the development of silicon integrated-circuit technology. Stable silicon dioxide provides an excellent interface to the silicon substrate and is important in both MOS and bipolar technology. As a result, the thermal oxidation of silicon has become an area of extensive research study, and much progress has been made in this field.

As the technology advances, through new structures and scaled-down existing devices, two-dimensional effects in silicon oxidation are becoming increasingly important. Greatly reduced oxide growth has been observed on the corners of silicon trenches and polysilicon. The highly nonuniform oxidation of two-dimensional nonplanar silicon structures plays a significant role in device isolation with trenches, SWAMI, or LOCOS, and in trench capacitors for high-density memory cells. It is also important in the oxidation of polysilicon involving double-poly, silicon on insulator, and oxide spacers in MOS devices. An understanding of this important subject has been limited by insufficient experimental data and difficulties in two-dimensional numerical simulation.

In this study, it will be quantitatively demonstrated that the oxidation of curved silicon surfaces is retarded at low temperatures and sharp curvatures, and that the retardation is more severe on concave than convex structures. This result is based on a unique experimental approach [2] – [4] in which extensive data were obtained concerning the oxidation of cylindrical silicon structures of controlled radii of curvature. These cylindrical structures were chosen because their symmetry facilitates analytical treatment and effectively reduces the physical modeling to one dimension.

This paper begins with a brief review of two-dimensional oxidation phenomena. Experimental procedures are then described in detail. The experimental results as characterized by surface curvature, oxide growth rate and viscosity will provide useful design guidelines. A theoretical model is developed in a separate paper [1] based on the premise that the viscous stress normal to the silicon surface is

responsible for the retarded oxide growth and that the stress in the bulk of the oxide accounts for the difference between concave and convex structures.

2 One-Dimensional Oxidation Effects

2.1 Results from One-Dimensional Oxidation

The one-dimensional thermal oxidation of silicon is described by the well-known Deal–Grove model [5] in which the new oxide is formed at the Si/SiO_2 interface and a steady state is maintained between oxidant diffusion through the oxide and chemical reaction at the interface. For relatively short oxidations, oxide thickness increases linearly with time. For relatively long oxidations, oxide thickness increases as a parabolic function of time. The growth rate decreases as the oxide becomes thicker, because the diffusion of oxidants through the existing oxide becomes the dominant factor in determining the growth rate.

The Deal–Grove model has one notable discrepancy; it does not predict the fast oxidation rate during the initial stages of dry O_2 oxidation. For thin-oxide growth, Massoud [6] developed a detailed experimental characterization and proposed an empirical model. The physics in the thin-oxide regime is still an area of research and controversy; however, it is widely believed that the stress at the Si/SiO_2 interface is responsible for the structural differences between the thin oxide and the bulk of the oxide.

2.2 Stress in Planar Oxidation

In the thermal oxidation of silicon, the new oxide is formed at the Si/SiO_2 interface. Because the volume of a silicon atom is only $20\mathring{A}^3$ and the volume of an oxide molecule is $45\mathring{A}^3$, volume expansion is necessary in the formation of the new oxide, and this requirement for additional volume leads to stress at the Si/SiO_2 interface as observed experimentally by EerNisse [7].

In his experiment, the back surface of the wafer was masked with a nitride

or thick oxide layer so that only the front could oxidize. During oxidation, the bending of the wafer was monitored by laser beams. At 950°C or lower the observed continuous increase in the curvature of the wafer as the oxide thickens is evidence of stress during oxide growth. Above 960°C, no change in the curvature during oxidation indicates that there is a viscous flow of oxide to relieve the stress.

For one-dimensional oxide growth, the Deal–Grove model was found to be adequate, which implies stress is implicitly included in its physical parameters. The stress effect, however, does have explicit applications in thin-oxide modeling; Irene [8] and Fargeix [9], among others, attempted to explain thin-oxide phenomena with models based on viscoelastic stress.

3 Two-Dimensional Oxidation Effects

In VLSI technology, many device structures involve the two-dimensional oxidation of nonplanar silicon surfaces. Oxide thickness is usually nonuniform, the silicon surface is often irregular, the electrical properties of the devices, such as breakdown voltage and leakage current, are severely impacted. Besides oxidant diffusion, stress and oxide flow now play critical roles, as will be demonstrated in the following examples.

3.1 Gate-Oxide Thinning

Transmission electron microscopy of MOS test devices [10] indicates that a thinning of the gate oxide can occur in a region close to a field-oxide wall. The amount of thinning is related to the angle between the isolation oxide wall and the horizontal surface at the base. Steeper walls produce a greater amount of thinning; as much as 20 to 30 percent have been observed. This phenomenon is not to be confused with the white-ribbon effect [11] in which residual silicon nitride at the edges of the field oxide prevents further growth of the gate oxide in a LOCOS structure.

It was conjectured that gate-oxide thinning is the result of the field oxide serving as a partial diffusion barrier that limits the oxidation rate locally. Numerical simulation [12] confirmed that the thicker field oxide could act as a partial barrier to oxidation simply because thick oxide grows slower than thin oxide. This barrier to diffusion, however, could account for only one-third of the gate oxide thinning. It was proposed that the additional thinning could be the result of stress effects on the surface reaction rate coefficient k_s or the solubility of the oxidants C^*.

3.2 Modeling of LOCOS Oxide Profile

Local oxidation (LOCOS) has been the most important approach for device isolation wherein a nitride mask is used to prevent oxidation in certain regions. There is always an oxide encroachment, however, that extends under the nitride. Early modeling was based on overly simplified assumptions and achieved only limited success. Significant progress was made when Chin [13] used two-dimensional numerical simulations to demonstrate that viscous flow is an important factor of nonuniform oxidation in addition to the oxidant diffusion. He was able to produce realistic LOCOS profiles and to calculate the components of viscous stress during oxidation.

Matsumoto and Fukuma [14] developed a numerical model that accounted for the elasticity of both nitride and oxide and described oxide motion and nitride bending as viscoelastic deformations. This formulation made possible the calculation of the shear component of the stress vector at the Si/SiO_2 interface which may contribute to the generation of defects. Elaborate numerical techniques were employed, and the resulting simulated oxide contours compared favorably to the experimental profiles after wet oxidation at 1000°C.

In both numerical models, stress was a driving force for the viscous flow of oxide but was not considered to affect the oxide growth rate. Discrepancies between the experimental and simulated results prompted speculation on the possibility that the oxidation rate at the Si/SiO_2 interface could be retarded by stress.

3.3 Corners of Silicon Trenches

Marcus and Sheng [15] produced dramatic examples of oxide thinning at the corners of silicon steps. TEM micrographs revealed a reduction up to 30 percent in oxide thickness at the edges of the steps following 900° and 950°C oxidations. Qualitatively, the suppressed oxidation at the concave corners was attributed to the decrease in oxidant supply because of the reduced exposure to the ambient at the corners. It was conjectured that the slower growth at convex corners could be the result of a reduction in diffusivity or solubility by compressive stress in the oxide. This argument is not valid, however, because the stress in convex oxide is tensile, as demonstrated in the physical model.[1].

Yoshikawa [16] investigated the effect of substrate doping on the shape of dry oxide grown on the corners of 1 μm deep silicon trenches at 900° to 1000°C. The following results were obtained.

- The shape and thickness of the oxide at the convex corner depend on phosphorus concentration and oxidation temperature.
- Sufficient phosphorus doping reduces thinning at the corners. This critical doping level is higher at lower temperatures.
- At concave corners, thinning occurs during the initial stage and cannot be prevented by heavy doping.

Yoshikawa proposed that the surface reaction rate constant k_s should be reduced by the strain energy of the elastic deformation of oxide. Using simplified numerical and physical formulations, he demonstrated the plausibility of reducing k_s by stress.

Hsueh and Evans [17] solved viscoelastic equations describing oxide deformation in cylindrical coordinates based on elaborate mechanical and mathematical treatments. As the authors noted, the effects of elastic strain and stress were overestimated and their theoretical results were inconsistent with known experimental observations.

3.4 Oxidation of Polysilicon

The oxidation of polysilicon gates has been widely applied in silicon processing technology. The insulating oxide between double layers of polysilicon is used in CCD and EPROM devices. In the LDD structure, the polysilicon gate is often oxidized to form sidewall spacers.

Rovedo [18] studied the oxidation of polysilicon for the double-poly process and developed a large collection of SEM profiles of oxides grown on polysilicon gates. One of his findings is that doping the polysilicon before etching results in polysilicon bending, sharp gate corners, and overhanging oxide, but doping after etching prevents these problems. Marcus [19] and Bravman [20] reported TEM studies of oxidized polysilicon surfaces. The observed irregularities (asperities, protuberances, bumps) are undesirable because they lower the breakdown voltage by increasing the local electric field. A model of the microscopic phenomena involves not only geometric effects, but also polysilicon grain growth and dopant segregation into the grain boundaries [20].

4 An Earlier Experiment To Characterize Stress

The first step to understanding two-dimensional oxidation is to characterize quantitatively the effects of stress on the oxide growth rate. This section describes the first experiment in this investigation designed to characterize stress. Based on the knowledge [7] that stress in a growing oxide could lead to the bending of the wafer, an experiment was carried out in this investigation to examine the assumption that wafer bending caused by the oxide on the back surface might exert compressive stress on the front side and that, if the back of the wafer was masked with varying amounts of oxide, the oxidation rate on the front side might exhibit observable changes. The experiment began by oxidizing n-type 11 to 20 Ωcm wafers in steam at 900°C for 12 hr to grow 8000 Å of thermal oxide on both sides. The frontside oxide was first etched off by HF. The wafers were then immersed in buffered HF for

different lengths of time to remove the oxide on the back. At this stage, the four groups of wafers ready for the oxidation-rate experiment were those with

- 8000 Å oxide on the back
- 4000 Å oxide on the back
- oxide completely etched off the back
- no oxide on the back (new wafers)

These wafers were oxidized in dry O_2 at 900°C for two hours. The thicknesses of the oxides were measured by a Nanospec optical interferometer, and no variations were observed. One possible explanation is that the bending caused by the back oxide did not generate sufficient stress to affect the oxidation rates on the front. The interaction of the interfacial stress from oxide growth and the mismatch in thermal-expansion coefficients is less clear.

5 Experiments in Two-Dimensional Oxidation

In this section, a unique experimental approach [2,4] is developed to obtain data concerning the retarded oxidation of cylindrical structures of varying radii of curvature. This approach was chosen because the symmetry of the cylindrical test structures will greatly simplify theoretical analysis of the experimental results.

5.1 Experimental Procedures

Cylindrical silicon structures of varying radii and thicknesses, with mask dimensions as small as 1 μm, were anisotropically etched in a silicon substrate. These cylindrical silicon walls and trenches were oxidized at temperatures ranging from 800° to 1200°C in both wet and dry ambients and under undoped and heavily doped conditions.

Figure 1 illustrates the processing sequence. Figure 1a shows a cylindrical ring of silicon anisotropically etched to a height of 3 μm, and Fig. 1b is its vertical cross

section and top view. In Fig. 1c, the ring is oxidized and covered with a layer of polysilicon, and the structure is then lapped down in Fig. 1d to expose the middle section of the silicon wall. Oxide thickness could now be measured by SEM. The polysilicon was used to protect the structure against lapping damage and to provide contrast in the micrographs.

Each experimental step is further described in the following sections.

5.2 Test Patterns and Mask Design

The most pronounced reduction in oxide growth occurs at the corners of the silicon structures. These corners are often observed, but they are two-dimensional and difficult to measure and characterize. An additional problem is the lack of experimental data based on controlled structural variations. To overcome these difficulties, the well-developed planar lithography technology was chosen to etch various test structures of controlled dimensions in the silicon substrate. The test patterns include concentric circles, isolated cylinders and holes, sharp angles, and rectangular structures. The rectangular structures provided corners as references; sharp corners with varying angles further illustrated the corner effects. Trenches of different widths and spacings were placed on the perimeter as references for process monitoring. The most important were the cylindrical structures with controlled radii, because they provided the experimental data for theoretical analyses in cylindrical coordinates. They were clustered in a 2 × 3 mm area to reduce variations in lapping, as will be discussed later. Thick stripes around these fine patterns would produce thick silicon walls as a protection against lapping damage.

On the mask, the smallest diameters were 1 μm and the sharpest angles were 4°. These small sizes presented severe challenges in the lithographic process of pattern transfer. On the chromium mask constructed by the electron beam, straight lines and sharp edges were reproduced successfully, but small 1 μm circles and holes became notably distorted. The first source of distortion stemmed from the pattern generation software that decomposed a circle into 0.25 μm trapezoids, and the re-

sultant polygon did not then resemble a circle. This problem could be prevented by improving the software if there should be a need for optimized circular structures. Further distortion probably occurred during pattern transfer to the chromium mask plate. The dots appeared smaller on the chromium plate than in the mask drawings, and the holes appeared larger, most likely the result of overetching in the chromium plate.

Positive photoresist AZ1470 was patterned by ultraviolet light, using a Canon FPA-141F 4:1 projection aligner. During the exposure and development of the photoresist, it was virtually impossible to obtain good photoresist patterns of small dots and holes simultaneously; small dots were susceptible to overexposure, and small holes were often underexposed. It was apparent that an optimal condition must be determined by trial and error.

5.3 Etching, Oxidation, and Polysilicon Deposition

Anisotropic dry etching of the silicon substrate took place in a Drytek DRIE-100 plasma etching system operated in the low ion-energy plasma etch mode. Highly anisotropic etching of silicon with good selectivity and fast etching rates was obtained with a mixture of SF_6 and C_2ClF_5 with a photoresist mask. This etch rate increase with the addition of SF_6 was the result of a rise in atomic fluorine in the plasma, and the anisotropy was related to the masking photoresist which releases hydrocarbons that polymerize in the presence of active species in the plasma [21]. The polymer layer on the sidewalls of the trench prevents further lateral etching, and the polymer on the bottom surface is removed by ion bombardment from the plasma which enables etching in the vertical direction. The polymers on the sidewall decompose in the air and are completely removed by the standard RCA cleaning process.[5] Such plasma etching had no effect on the oxide thickness obtained from subsequent oxidation [22].

[5](a) 5:1:1 H_2O:H_2O_2:NH_4OH at 70°C, 10 min, (b) DI water rinse, (c) 5:1:1 H_2O:H_2O_2:HCl at 70°C, 10 min, (d) DI water rinse, (e) 50:1 HF for 30 sec, and (f) DI water rinse.

The etching profiles were found to be a function of total gas flow and pressure [21]; higher flows reduced bowing on vertical surface, and lower pressure minimized undercutting. The etching rate of the silicon substrate was approximately 6.5 min for 1 μm, with a gas flow of 175 sccm each for SF_6 and C_2ClF_2, a pressure of 130 mTorr, and an RF power of 500 W. The structures were etched to a depth of 3 μm so that they were not too high and fragile to survive lapping but were long enough to create a uniform section away from the edges. Figure 2a is an SEM micrograph of the as-etched concentric rings.

The oxidation was carried out over a wide range of temperatures and at times chosen to grow the same amount of oxide on flat surfaces at all temperatures – nominally 5000 Å for wet and 3500Å for dry oxidations. These conditions were selected to produce sufficiently thick oxides for measurement and to avoid excessively long oxidations. As a protective layer over the oxide, a 1 μm LPCVD polysilicon was deposited at 620°C and at a pressure of 500 mTorr for 90 min. Figure 2b shows the concentric test structures after polysilicon coating.

5.4 Lapping

A critical step in the experiment was the search for a process to remove the top half of the cylindrical structure to reveal the shape of the oxide at the center, which would be free from the irregularities near the top and bottom corners. Because silicon, polysilicon, and SiO_2 were involved, a nonselective etching mechanism would be required. Ion milling was considered but not selected because of its expense and low throughput. Plasma and chemical etching processes were investigated, but the search for a good combination of etching steps proved futile because the development of VLSI processing has forced chemical and plasma etching toward high selectivity. The failure to identify a suitable etching process led to the apparently imprecise procedure of mechanical lapping.

The damage caused by mechanical lapping became a serious problem. A 1 μm layer of polysilicon was required to provide adequate support and clear contrast.

An additional challenge was to ensure the same lapping depth over a reasonably wide sample area so that all the test structures could be compared under the same condition. Horizontal lapping was extremely difficult to achieve over a large area; there was always uncontrollable slanting in the surface, apparently as a result of the inherent imprecision in the manual and mechanical process of lapping. It would be a rare achievement to limit the depth variation to 1 μm over a 3000 μm wide area. To minimize the variations caused by lapping, test patterns in the mask were clustered in a small 2 $\times$ 3 mm area.

5.5 Measurements

After lapping, the samples were ready for oxide-thickness measurement by means of a scanning electron microscope (SEM), chosen because of its reasonable resolution and relative ease of use [23].

A typical high-magnification SEM micrograph for the oxide-thickness measurement consisted of a band of oxide sandwiched between regions of polysilicon and silicon. An attempt to make use of the difference in emission efficiencies between the oxide and silicon was not successful; the low contrast was inadequate for the oxide-thickness measurement, and the task of locating test patterns became much more difficult.

To resolve the contrast problem, the oxide was etched off to produce a trench between the silicon region and polysilicon layer. The lapped samples were first immersed in 6:1 buffered HF for several minutes to etch out the oxide, and a 100 Å layer of gold was then sputtered over the sample to take advantage of the high electron emission rate of gold. These additional steps provided excellent contrast in the SEM image, as shown in Figs. 2c. The space vacated by the oxide now appeared as a dark strip sandwiched between two bright areas of silicon and polysilicon.

For the oxide-thickness measurement, micrographs were taken at magnifications of $\times$20,000 to $\times$50,000, and the regions to be measured were centered to avoid distortion. The highest useful magnification was $\times$50,000; any higher did not improve

the resolution which was probably limited by the test structures themselves. To improve resolution, brightness and contrast were greatly reduced. In addition, focusing was carried out from a point near the target region to protect the true target from excessive exposure to the electron beam.

6 Experimental Results

In a two-dimensional silicon structure, crystal orientation varies. The implications of the different crystal orientations on the surface of a cylinder are discussed in this section, and new data concerning oxide growth on the ⟨110⟩ orientation are reported. The results obtained from retarded oxidation for wet and dry oxides and the effects of doping are also discussed.

6.1 Crystal Orientation

It is well known that the oxidation rate of silicon is a function of the crystal orientation of the silicon surface [22,24]. The parabolic rate constant B is independent of substrate orientation; however, the linear rate constant B/A shows a clear dependence on crystal orientation. It has been reported [24] that the ⟨100⟩ orientation has a lower growth rate than ⟨111⟩,

$$\left(\frac{B}{A}\right)_{\langle 111\rangle} \approx 1.68 \times \left(\frac{B}{A}\right)_{\langle 100\rangle} \tag{1}$$

On the other hand, the relative magnitudes of growth rates in the ⟨110⟩ and ⟨111⟩ surfaces appear to vary with temperature and ambient[24]. Table 1 lists the results of this study. The ratios of wet-oxide thickness on the flat ⟨110⟩ and ⟨100⟩ surfaces have been determined from oxides on trench sidewalls of respective orientations. The thickness of the oxide on the ⟨100⟩ surface was determined by an optical interferometer. Based on the Deal–Grove model, the best fit for wet oxide is achieved by

$$k_{s\langle 110\rangle} \approx 1.45 \times k_{s\langle 100\rangle} \tag{2}$$

Table 1: CONDITIONS FOR WET PLANAR OXIDATION

Temperature	800°C	900°C	1000°C	1100°C	1200°C
Time(min)	1440	300	96	40	24
$t_{ox(100)}$(Å)	5027	4575	4735	4880	5554
$\frac{t_{ox(110)}}{t_{ox(100)}}$	1.29	1.25	1.18	1.05	1.03

In a cylindrical structure, crystal orientation varies along the circumference periodically, as illustrated in Fig. 3 and, under oxidation conditions where the orientation effect is important, oxide thickness also varies periodically, as shown in Fig. 3c. To be consistent, the characterization of retarded oxidation was based on oxide thicknesses measured on the ⟨110⟩ surface and normalized to the oxide thickness on the flat ⟨100⟩ vertical wall, which was calibrated to the oxide thickness on the ⟨100⟩ wafer surface as determined by a Nanospec optical interferometer.

6.2 Wet Oxidation

The experiments with wet oxides were conducted at temperatures ranging from 800° to 1200°C, and the conditions are listed in Table 1. The experimental results are best illustrated by SEM micrographs. Figure 4a is the result of oxidation at 800°C in steam. The dark band is the oxide; silicon is on one side, and polysilicon is on the other. The oxide is 5000 Å thick on the straight surface and is much thinner at the corners. At 1100°C (Fig. 4b), the oxide on the straight surface is again 5000 Å thick; here, the oxide thickness is fairly uniform, and the silicon corners are well rounded.

The most useful data for quantitative analysis are based on cylindrical structures with well-defined radii of curvature. Figure 5 describes the temperature effects on small cylinders at higher magnifications, and oxidations at 800° and 1100°C are compared. The oxides on the straight surfaces have the same thicknesses; on the curved surfaces, however, they are thinner at 800°C than at 1100°C, which is direct

evidence of the retardation of oxide growth at low temperature and small radius.

Figure 6 compares oxides on a convex and concave silicon surface. On the right is a silicon cylinder with oxide grown on its outer (convex) surface, and on the left is a hole etched in the silicon with oxide grown on its inner (concave) surface. Note that the oxide on the concave surface is thinner. Furthermore, the concave corner also grew thinner oxide, although it is not as sharp as the convex corner.

These observations are plotted in Fig. 7. The vertical axis measures oxide thickness on curved surfaces normalized to that on the flat surface ($\approx$ 5000 Å for all temperatures). The horizontal axis denotes the inverse of the radius of curvature after oxidation, with the flat surface at the origin and the smaller radii to the right. The straight lines are the least-mean-square fit to the data points and indicate the trend of the data; the solid lines are convex structures (cylinders) and the dotted lines are concave structures (holes). Figure 8 is a magnified plot of the oxidation data for concave surfaces.

The major results of this experiment are summarized as follows:

- Oxide thickness is a strong function of the radius of curvature of the silicon surface; the smaller the radius, the thinner the oxide. Because the radii in all plots are as measured from the SEM micrographs, they represent the radii of the silicon surfaces after oxidation. The smallest cylinder observed has a radius of approximately 1200 Å.

- The retardation of oxidation is more pronounced at lower temperatures, as indicated by the steep slopes of the straight lines in the 800° and 900°C data; it is less severe at higher temperatures and is not observable at 1200°C.

- This dependence on temperature and radius also holds true for concave surfaces. As a group, however, retarded oxidation is much more severe than in convex surfaces; suppressed oxidation was observed in concave silicon surfaces with a radius of curvature as large as 10 μm and at temperatures as high as 1100°C.

These well-defined characteristics will form the basis of the theoretical model [3,4] in which the retarded oxide growth is attributed to the reduced chemical reaction rate at the interface due to viscous stress, and the different stresses in the

bulk of the oxide (compressive for concave and tensile for convex surfaces) account for the thinner oxides on the concave structures. The temperature dependence of the retardation is mainly determined by that of the oxide viscosity which is higher at lower temperatures and, as a result, the stress is higher at lower temperature, leading to more retardation. The more severe retartdation for smaller radii is the result of higher stress produced by more drastic deformation of the oxide having a small radius of curvature. This model will be described in detail in a separate paper [1].

Additional features in the experimental data are also worth noting. First, enhanced oxidation is observed on convex surfaces of 1–2 μm radii; they are slightly thicker than oxides on flat surfaces. Second, the temperature dependence of the oxides on concave surfaces is reversed for 800° and 900°C. These subtle points will be addressed following the development of the physical model[1].

6.3 Dry Oxidation

The cylindrical test structures were also oxidized in dry oxygen at at temperatures ranging from 900° to 1200°C and for times long enough to grow nominally 3500Å oxide on flat surfaces. Oxidation at 800°C was neglected because it would have required 500 hr to grow the desired thickness for measurement.

A representative SEM micrograph of dry oxidation is shown in Fig. 9, and experimental results are plotted in Fig. 10 for normalized oxide thickness versus the inverse of the radius of curvature. It can be seen that retardation in oxide growth is more severe at lower temperatures, for smaller radii, and on concave surfaces. Slightly enhanced oxidation is also observed on convex surfaces of $1 - 2$ μm radii. Qualitatively, they are similar to the results obtained from the wet oxidations, but the retardation appears to be more severe.

6.4 Doping Effects

In device fabrication, it is often necessary to oxidize doped silicon structures. The effect of doping on one-dimensional oxidation has been reported in the literature [25]. Impurity doping in the substrate changes the oxidation rates, and the dopants segregated into the oxide affect the bulk properties of the oxide. Experiments using doped wafers were developed as part of this study to investigate the doping effects on two-dimensional oxidation. The results are illustrated in Fig. 11 where the normalized oxide thicknesses are plotted against the inverse of the radius of curvature for three groups of test structures oxidized in steam at 900°C. The oxidation conditions were chosen such that the straight surfaces grew approximately 5000 Å of oxide. In the undoped structures, oxide growth was severely retarded. The deglazed group was heavily doped in a $POCl_3$ furnace for 60 min at 950°C, deglazed to remove the 800 Å phosphosilicate glass, and then oxidized; the retardation behavior was similar to the undoped wafers, although the doped structures was oxidized for only 20 min instead of the 5 hr required for the undoped wafers. The not-deglazed group was heavily doped and then oxidized with the layer of phosphosilicate glass retained; much less retardation was observed.

The experimental data obtained for doping effects can be explained qualitatively by the physical model based on viscous stress[1], in which the stress is determined by the product of the growth rate and oxide viscosity, both of which are changed by impurity doping. In the doped-deglazed group (which was heavily doped, deglazed to remove the phosphorus glass, and then oxidized), the growth rate is greatly enhanced by doping, but the viscosity of the oxide is reduced by the dopants segregated into the oxide. These two mechanisms cancel each other, and the doped-deglazed group exhibits severe retardation similar to that of the undoped group, even though the oxidation time for the deglazed group was only 20 min, whereas the undoped group required 5 hr. The doped-undeglazed group also had a much enhanced growth rate and the potential for high stress, but the large amount of dopants retained in the phosphorus glass during oxidation helped to reduce the viscosity of the oxide

to an even greater extent and, as a result, retardation is minimized.

7 Summary

A unique experimental procedure was introduced in this paper. Silicon structures of various shapes were formed on a silicon substrate by anisotropic dry etching. They were oxidized, covered with a layer of LPCVD polysilicon, and then lapped back to reveal the shapes and thicknesses of the oxide. Both wet and dry oxides exhibit similar characteristics. Oxide thickness is a strong function of the radius of curvature of the silicon surface; the smaller the radius, the thinner the oxide. The suppression of oxidation is more pronounced at lower temperatures and on concave surfaces and is less severe at higher temperatures and on convex surfaces.

In addition, experiments with heavily doped structures indicated that retaining the phosphosilicate glass after doping was very effective in reducing the retardation of oxide growth. These experimental results will serve as a basis for theoretical analysis and modeling [1], in which viscous stress plays a dominant role.

Many possible new applications of the methodology based on cylindrical test structures offer the advantages of simplified analysis and a unique means of producing high stress during oxidation. These cylindrical structures can be used to investigate stress in different types of oxidation and annealing processes, such as low-temperature, high-pressure, and plasma-enhanced oxidations. There are also potential applications in two-dimensional diffusion, interaction of oxidation and diffusion, and behavior of defects and interface states under stress.

To realize these potential applications, improved processing and analysis techniques will be required to overcome practical difficulties. First, measurement based on SEM has inadequate resolution for thin-oxide applications, and the resolution of TEM may become desirable. Smaller and more controllable cylindrical structures made possible by improved lithography and anisotropic etching are useful in characterizing high stress. Cylindrical structures enable analytical treatment[1] only if certain two-dimensional phenomena (such as crystal orientation effect) are ignored.

For more detailed analysis, numerical techniques will be needed.

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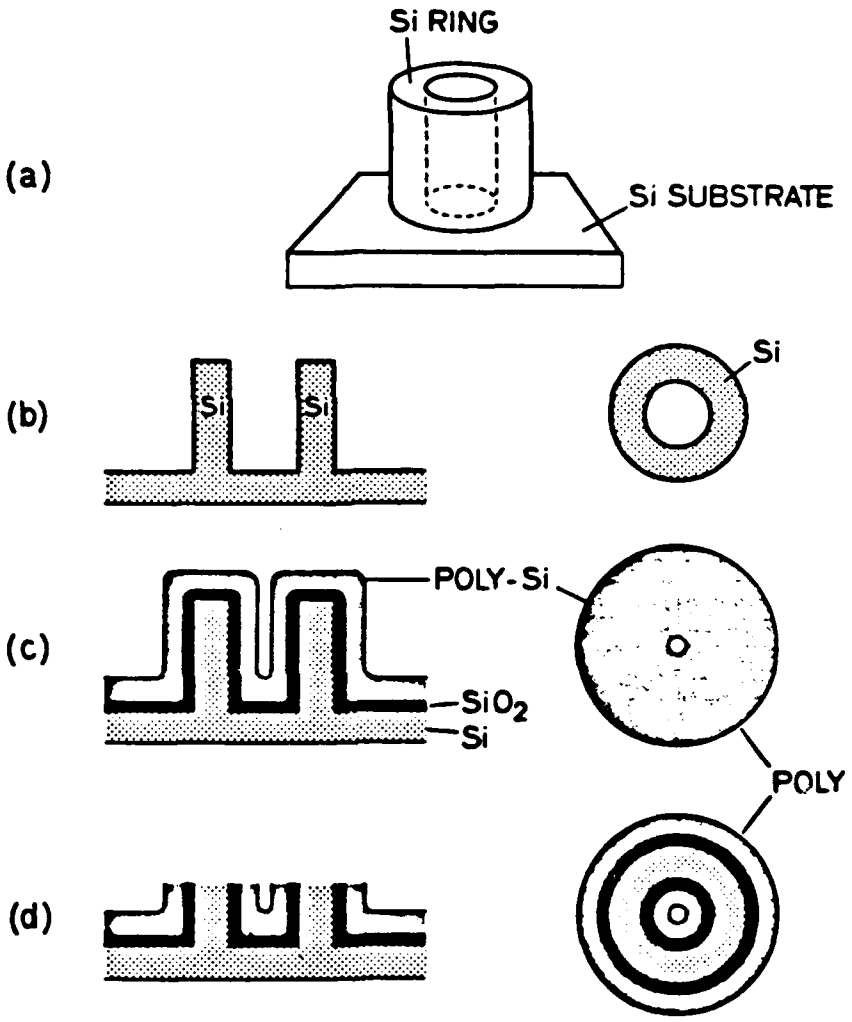

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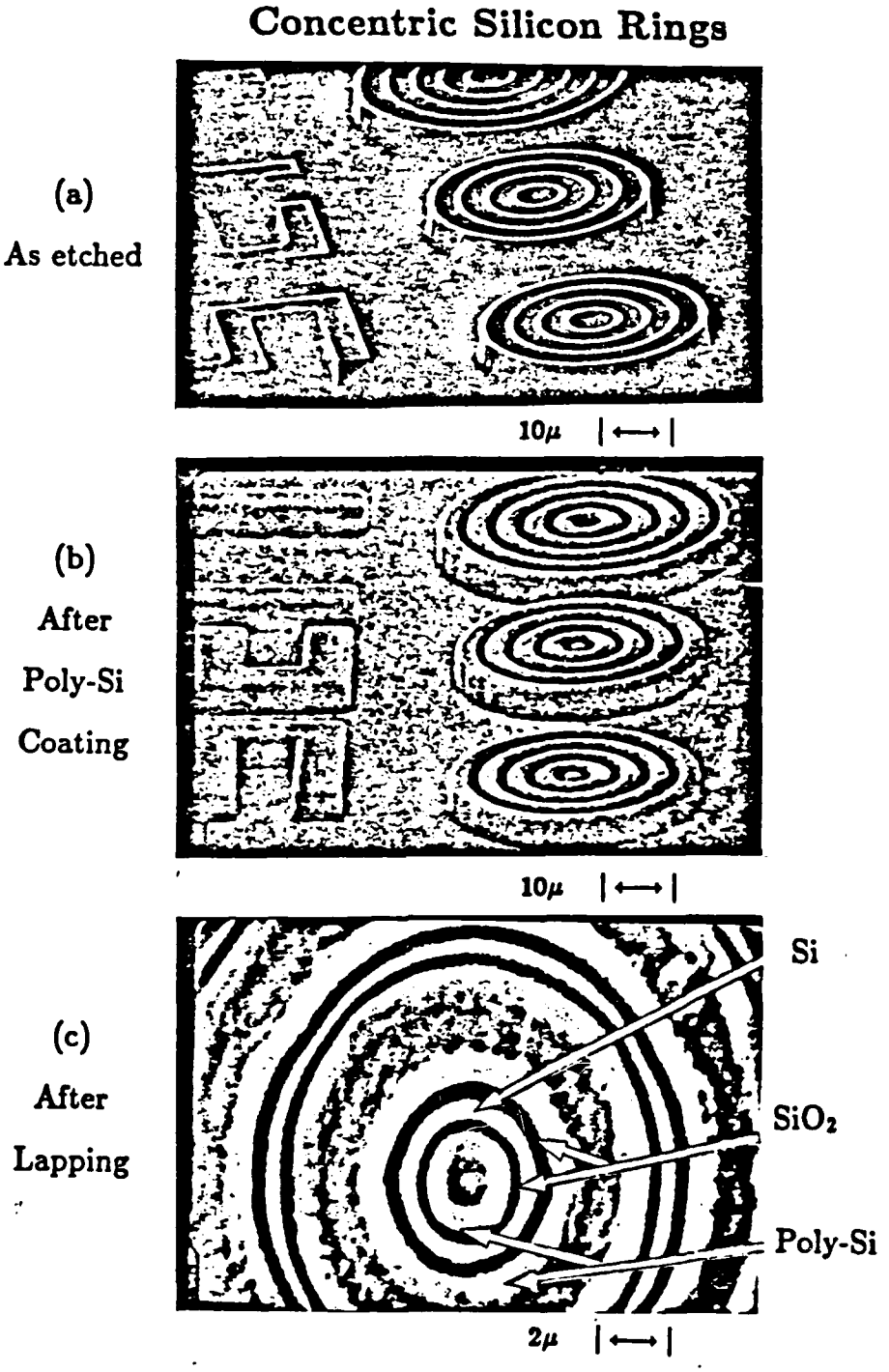

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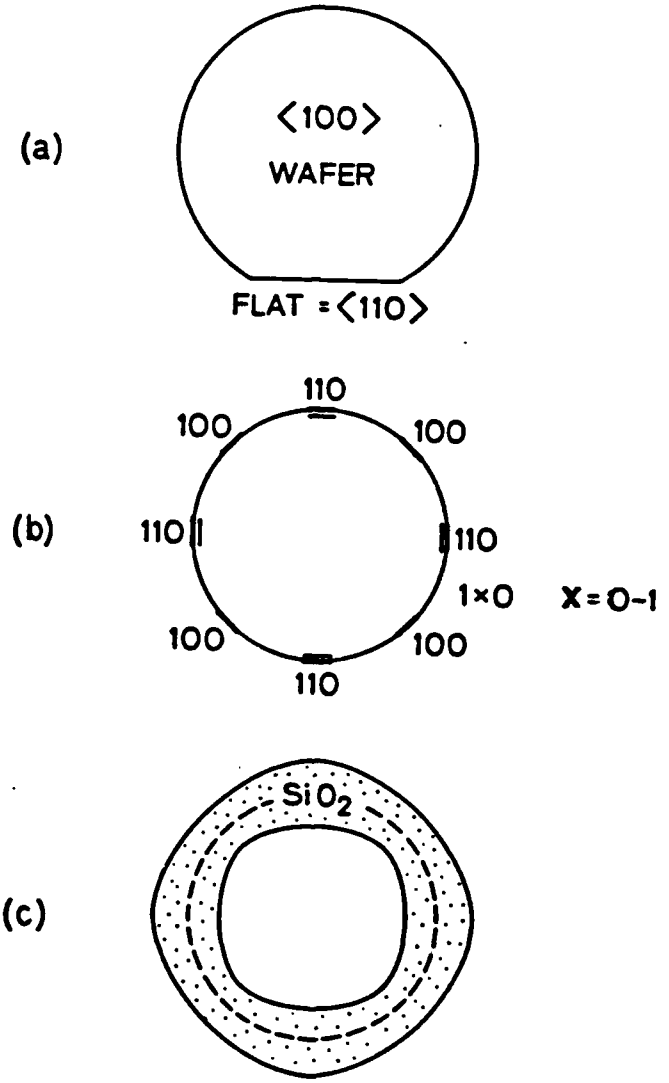

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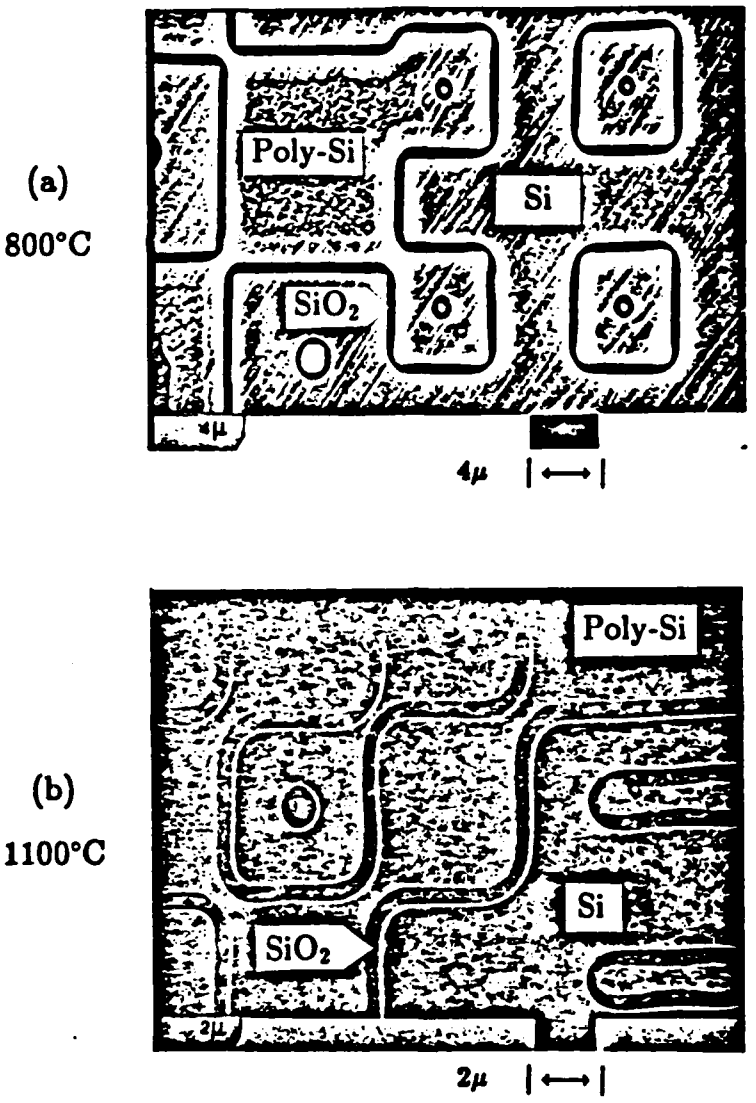

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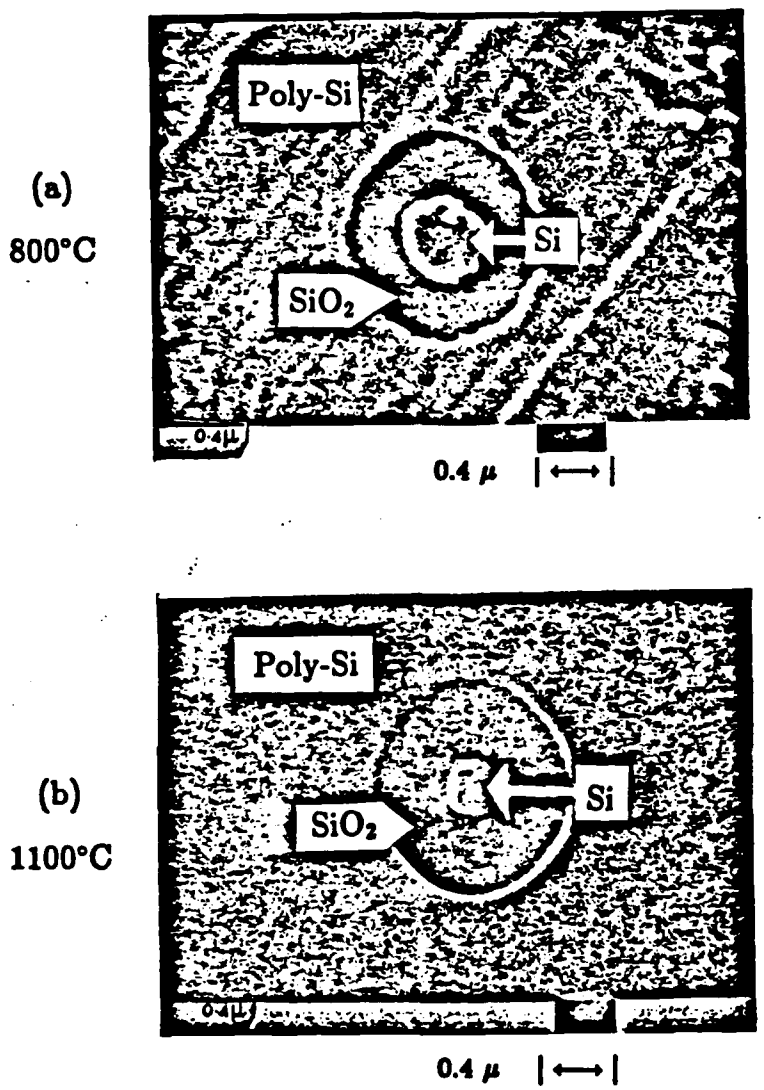

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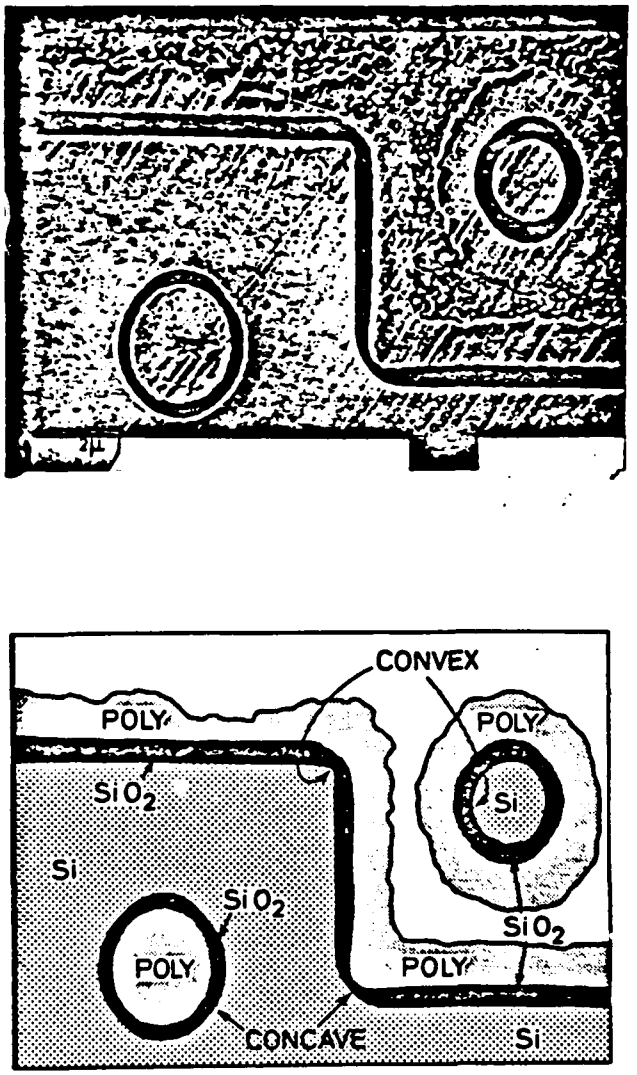

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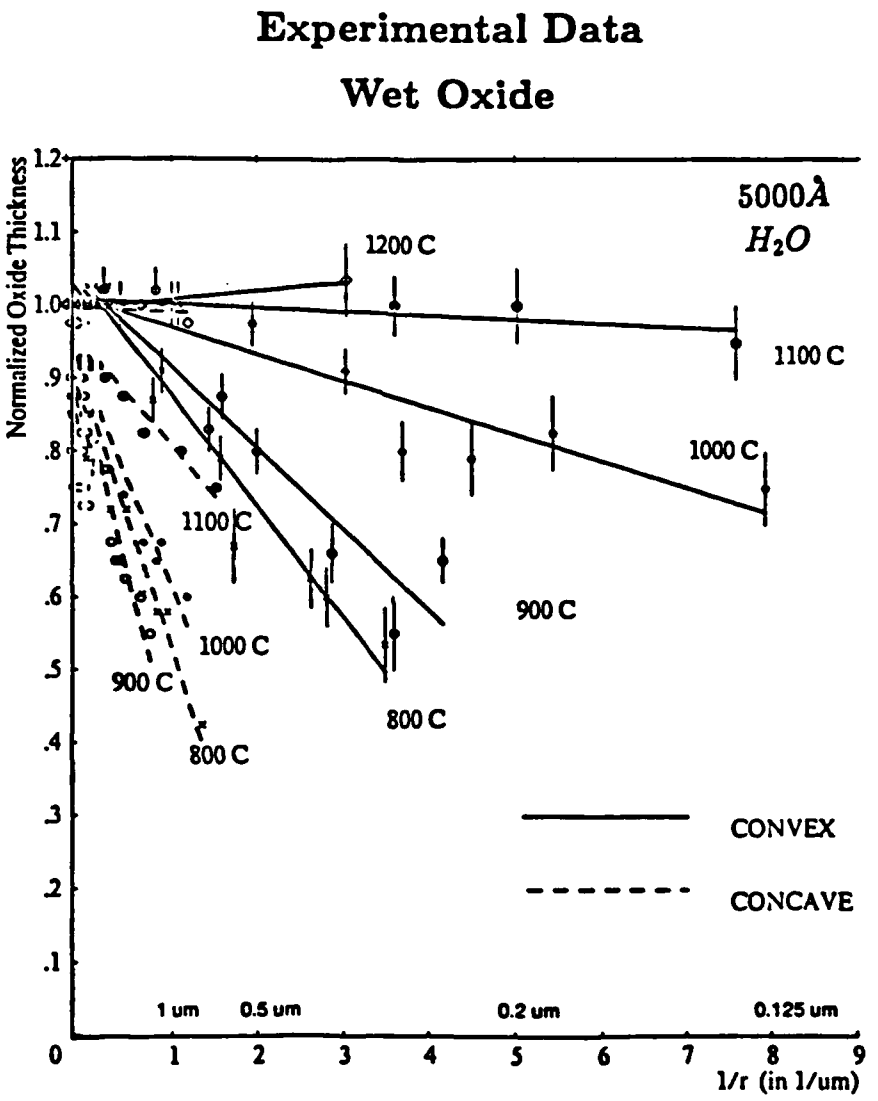

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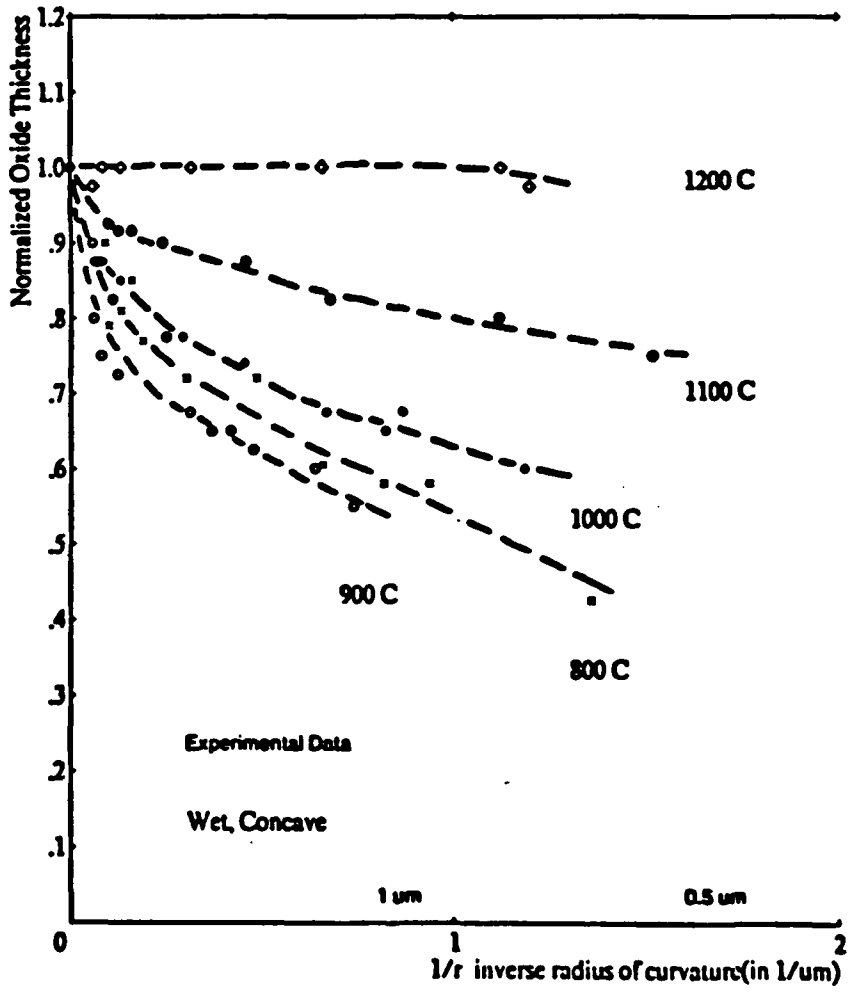

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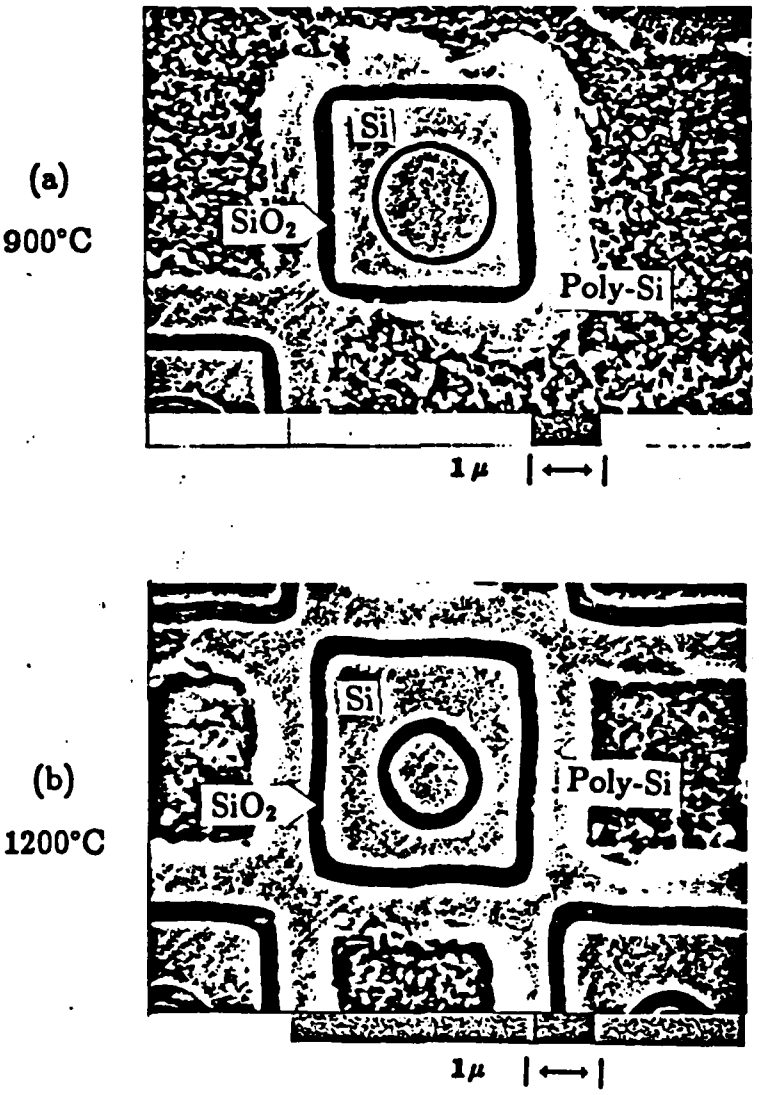
Dry Oxide



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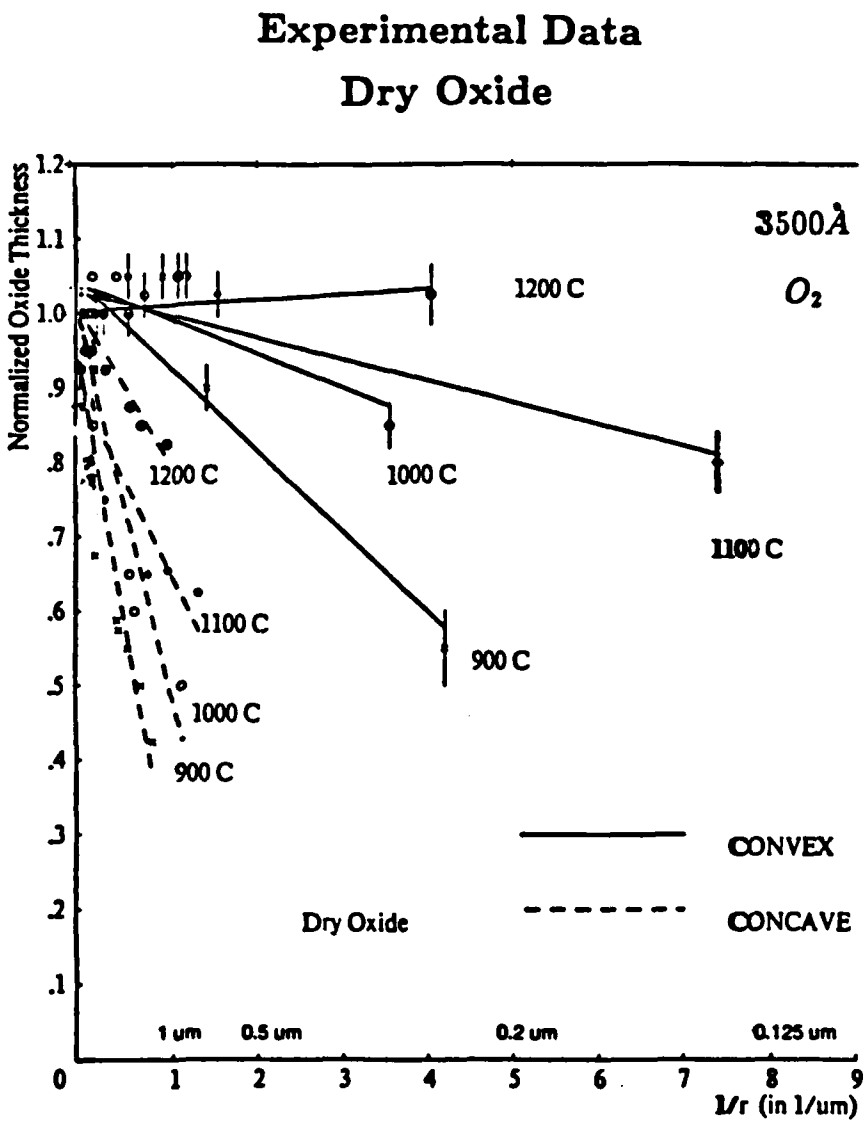

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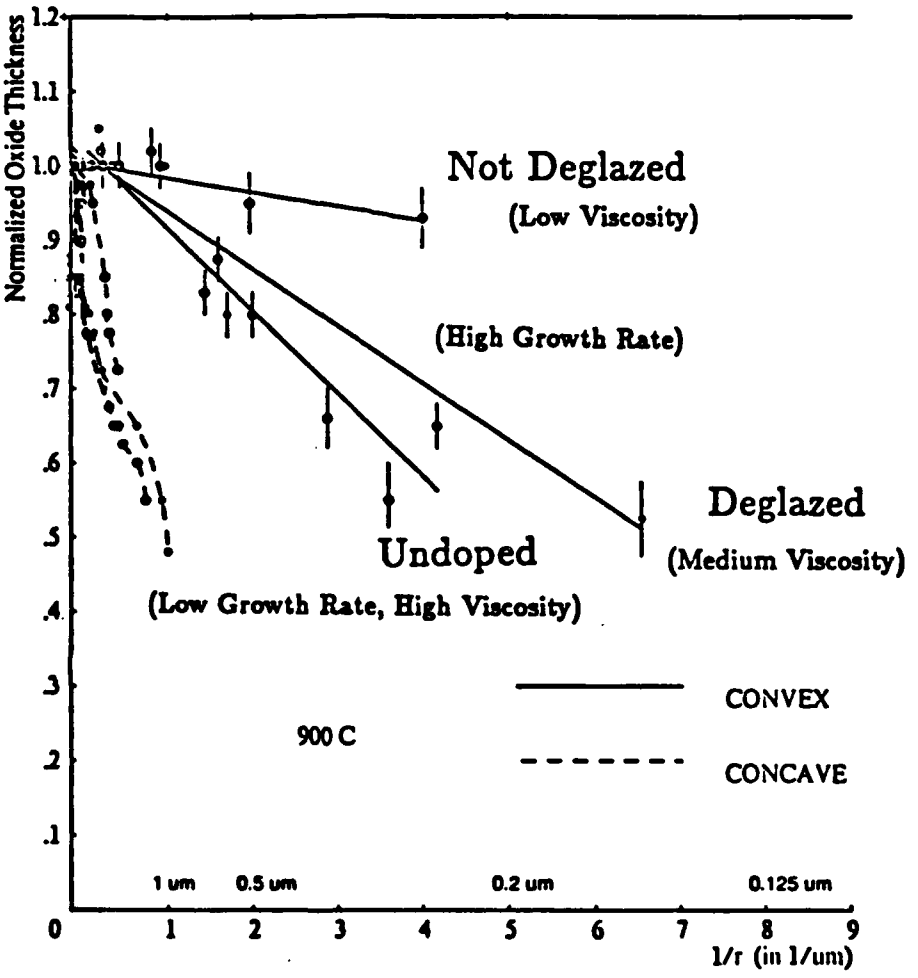

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